CLAIMS:

1. A data processing device (100; 100') having at least one microprocessor (90) and having at least one additional arithmetic unit (40) for performing at least one particular defined calculation, the arithmetic unit 40 being coupled to the microprocessor (90) via a number of registers, of which first registers are provided for controlling the data transfer and second registers are provided for transmitting commands, characterized in that the registers may be loaded from at least one particularly peripheral memory (10), for example

- from at least one R[andom]A[ccess]M[emory],
- from at least one R[ead]O[nly]M[emory] or
- from at least one E[lectrically] E[rasable] P[rogrammable] R[ead] O[nly] M[emory].

2. A data processing device as claimed in claim 1, characterized in that at least one set of temporary registers (20, 22, 24, 26, 28) is assigned to the memory (10), which set of registers is connected (230, 232, 234, 236, 238) to at least one set of main registers (30, 32, 34, 36, 38) assigned to the arithmetic unit (40) and intended for storage of the registers for the active calculation.

3. A data processing device as claimed in claim 1 or claim 2, characterized in that the memory (10) may be acted upon (170) by at least one address register (70) intended for pointing to the start address of the data to be loaded, which address register (70) is connected (670) to at least one control logic circuit (60).

4. A data processing device as claimed in claim 3, characterized in that assigned to the arithmetic unit (40) is at least one control register (50), which is connected (560) to the control logic circuit (60).

5. A data processing device as claimed in claim 3 or claim 4, characterized in that at least one counting register (72) for indicating the register sets to be loaded in sequence is assigned (672) to the control logic circuit (60).

6. A data processing device (100') as claimed in at least one of claims 1 to 5, characterized in that at least one selection circuit (74) is connected between the set of temporary registers (20, 22, 24, 26, 28) and the set of main registers 30, 32, 34, 36, 38), for combination with at least one set (a, b, c) of registers (80, 82, 84, 86, 88) assigned to the microprocessor (90).

7. A data processing device as claimed in claim 6, characterized in that the selection circuit (74) may be acted upon by at least one bit position (51, 52, 53, 54) of the control register (50).

8. A portable data carrier having at least one data processing device (100; 100') as claimed in at least one of claims 1 to 7.

9. A semiconductor chip comprising at least one integrated data processing device (100; 100') as claimed in at least one of claims 1 to 7.

10. A method of performing at least one particular defined calculation by means of at least one data processing device (100; 100') having at least one microprocessor (90) and having at least one additional arithmetic unit (40), characterized by the following method steps:

(i) initialization of at least one address register (70) and at least one counting register (72) by the microprocessor (90);

(ii) starting of the calculation by assertion of at least one control bit;

(iii) copying or loading of data beginning at the start address from at least one in particular peripheral memory (10) into at least one set of temporary registers (20, 22, 24, 26, 28);

(iv) incrementation of the address register (70) with each access to the memory (10);

(v) establishing whether the set of temporary registers (20, 22, 24, 26, 28) is complete:

(v.a) if the set of temporary registers (20, 22, 24, 26, 28) is complete (+), proceeding to method step (vi);

(v.b) if the set of temporary registers (20, 22, 24, 26, 28) is incomplete (-), proceeding to method step (iii);

(vi) establishing whether the arithmetic unit (40) is active:

(vi.a) if the arithmetic unit (40) is active (+), proceeding to method step (vi);

(vi.b) if the arithmetic unit (40) is inactive (-), proceeding to method step (vii);

(vii) copying or transferal of data from the set of temporary registers (20, 22, 24, 26, 28) into at least one set of main registers (30, 32, 34, 36, 38);

(viii) decrementation of the counting register (72);

(ix) starting of the calculation in the arithmetic unit (40);

(x) establishing whether the counting register (72) has been decremented to zero:

(x.a) if the counting register (72) has been decremented to zero (+), proceeding to method step (xi);

(x.b) if the counting register (72) has not been decremented to zero (-), proceeding to method step (iii);

(xi) termination.